

WHAT IS CLAIMED IS:

1. A current source comprising:

a first stage coupled to an input current source, the first stage containing circuitry to receive an input current provided by the input current source;

a second stage coupled to the first stage, the second stage comprising:

a first transistor and a second transistor serially coupled together, wherein a first terminal of the second transistor is coupled to a second terminal of the first transistor;

a third transistor having a first terminal coupled to a third terminal of the first transistor; and

a level shifter coupled to a third terminal of the third transistor and the first terminal of the second transistor, the level shifter containing circuitry to elevate a voltage at a third terminal of the second transistor, wherein the level shifter is arranged in a source-follower configuration.

2. The current source of claim 1, wherein the level shifter comprises a fourth transistor having a first terminal coupled to the third terminal of the third transistor and a third terminal coupled to the first terminal of the second transistor.

3. The current source of claim 2, wherein the first, second, and third transistors are N-type MOSFET (metal-oxide semiconductor field-effect transistors), and wherein the fourth transistor is a P-type MOSFET.

4. The current source of claim 2, wherein a first current source is coupled between a substrate power supply and the first terminal of the third transistor and a second current source is coupled between the substrate power supply and the first terminal of the fourth transistor.

1 5. The current source of claim 4, wherein the first current source provides a first current that
2 is approximately four times a second current provided by the second current source.

1 6. The current source of claim 1, wherein the level shifter comprises a plurality of
2 transistors coupled in parallel, wherein each transistor has a first terminal coupled to the third
3 terminal of the third transistor and a third terminal coupled to the first terminal of the second
4 transistor.

1 7. The current source of claim 6, wherein each transistor in the plurality of transistors are P-
2 type MOSFET (metal-oxide semiconductor field-effect transistors).

1 8. The current source of claim 6, wherein each transistor in the plurality of transistors have
2 identical geometries.

1 9. The current source of claim 1, wherein the first stage comprises:
2 a fifth transistor and a sixth transistor serially coupled together, wherein a first terminal
3 of the sixth transistor is coupled to a second terminal of the fifth transistor;
4 a seventh transistor having a first terminal coupled to a third terminal of the fifth
5 transistor; and
6 a second level shifter coupled to a third terminal of the seventh transistor and the first
7 terminal of the sixth transistor, the second level shifter containing circuitry to elevate a voltage at
8 a third terminal of the sixth transistor.

1 10. The current source of claim 9, wherein the second level shifter is arranged in a source-
2 follower configuration.

1 11. The current source of claim 9, wherein the second level shifter comprises an eighth
2 transistor having a first terminal coupled to the third terminal of the seventh transistor and a third
3 terminal coupled to the first terminal of the sixth transistor.

1 12. The current source of claim 11, wherein the fifth, sixth, and seventh transistors are N-
2 type MOSFET (metal-oxide semiconductor field-effect transistors), and wherein the eighth
3 transistor is a P-type MOSFET.

1 13. The current source of claim 11, wherein a third current source is coupled between a
2 substrate power supply and the first terminal of the seventh transistor and a fourth current source
3 is coupled between the substrate power supply and the first terminal of the eighth transistor.

1 14. The current source of claim 13, wherein the third current source provides a third current
2 that is approximately four times a fourth current provided by the fourth current source.

1 15. The current source of claim 9, wherein the first terminal of the fifth transistor is coupled
2 to the input current source.

1 16. The current source of claim 1, wherein the first terminal is a source terminal, the second
2 terminal is a drain terminal, and the third terminal is a gate terminal.

1 17. A current source comprising:

2 a first stage coupled to an input current source, the first stage comprising:

3 a first transistor and a second transistor serially coupled together, wherein a first
4 terminal of the second transistor is coupled to a second terminal of the first transistor;

5 a third transistor having a first terminal coupled to a third terminal of the first
6 transistor;

7 a second level shifter coupled to a third terminal of the third transistor and the
8 first terminal of the second transistor, the second level shifter containing circuitry to elevate a
9 voltage at a third terminal of the second transistor;

10 the current source further comprising a second stage coupled to the first stage, the second
11 stage comprising:

12 a fourth transistor and a fifth transistor serially coupled together, wherein a first
13 terminal of the fifth transistor is coupled to a second terminal of the fourth transistor;

14 a sixth transistor having a first terminal coupled to a third terminal of the fourth
15 transistor; and

16 a level shifter coupled to a third terminal of the sixth transistor and the first
17 terminal of the fifth transistor, the level shifter containing circuitry to elevate a voltage at a third
18 terminal of the fifth transistor, wherein the level shifter is arranged in a source-follower
19 configuration.

1 18. The current source of claim 17, wherein the level shifter comprises a seventh transistor

2 having a first terminal coupled to the third terminal of the sixth transistor and a third terminal

3 coupled to the first terminal of the fifth transistor and wherein the second level shifter comprises

4 an eighth transistor having a first terminal coupled to the third terminal of the third transistor and
5 a third terminal coupled to the first terminal of the second transistor.

1 19. The current source of claim 18, wherein the seventh and the eighth transistors have
2 identical geometries.

1 20. The current source of claim 17, wherein the level shifter comprises a plurality of
2 transistors coupled in parallel, wherein each transistor has a first terminal coupled to the third
3 terminal of the sixth transistor and a third terminal coupled to the first terminal of the fifth
4 transistor and wherein the second level shifter comprises a second plurality of transistors coupled
5 in parallel, wherein each transistor has a first terminal coupled to the third terminal of the third
6 transistor and a third terminal coupled to the first terminal of the second transistor.

1 21. The current source of claim 20, wherein each transistor in the plurality of transistors and
2 the second plurality of transistors have identical geometries.

1 22. The current source of claim 17, wherein the current source is used in a wireless device.

1 23. A current source comprising:
2 a first stage coupled to an input current source, the first stage containing circuitry to
3 receive an input current provided by the input current source;
4 a second stage coupled to the first stage, the second stage comprising:
5 a first transistor and a second transistor serially coupled together, wherein a first
6 terminal of the second transistor is coupled to a second terminal of the first transistor;
7 a level shifter coupled to a third terminal of the second transistor and a second
8 terminal of the first transistor, the level shifter containing circuitry to elevate a voltage at the
9 third terminal of the second transistor, wherein the level shifter is arranged in a source-follower
10 configuration; and
11 a third transistor having a third terminal coupled to the level shifter.

1 24. The current source of claim 23, wherein the level shifter comprises a fourth transistor
2 having a second terminal coupled to the third terminal of the second transistor and to the third
3 terminal of the third transistor.

1 25. The current source of claim 24, wherein the first, second, and third transistors are P-type
2 MOSFET (metal-oxide semiconductor field-effect transistors), and wherein the fourth transistor
3 is an N-type MOSFET.

1 26. The current source of claim 24, wherein a first current source is coupled between a
2 substrate ground and the fourth transistor.

1 27. The current source of claim 23, wherein the first terminal is a source terminal, the second
2 terminal is a drain terminal, and the third terminal is a gate terminal.